LAW OFFICES
SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
WASHINGTON, D.C. 20037-3202
TELEPHONE (202) 293-7060
FACSIMILE (202) 293-7860

CALIFORNIA OFFICE
1010 EL CAMINO REAL
MENLO PARK, CA 94025
TELEPHONE (650) 325-5800
FACSIMILE (650) 325-6606

August 10, 2000

JAPAN OFFICE
TOEI NISHI SHIMBASHI BLDG. 4F
13-5 NISHI SHIMBASHI 1-CHOME
MINATO-KU, TOKYO 105, JAPAN
TELEPHONE (03) 3503-3760
FACSIMILE (03) 3503-3756

BOX: PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Application of **Shinsuke YOKOKAWA**
PROGRAMMABLE CONTROLLER
Our Reference: Q60393

Dear Sir:

Attached hereto is the application identified above including the specification, claims, executed Declaration and Power of Attorney, four (4) sheets of drawings, one (1) priority document, executed Assignment and PTO Form 1595.

The Government filing fee is calculated as follows:

Total Claims	3 - 20 =	0 x $18 =	$ 000.00
Independent Claims	1 - 3 =	0 x $78 =	$ 000.00
Base Filing Fee	($690.00)		$ 690.00
Multiple Dep. Claim Fee	($260.00)		$ 000.00
TOTAL FILING FEE			**$ 690.00**
Recordation of Assignment Fee			$ 40.00
TOTAL U.S. GOVERNMENT FEE			**$ 730.00**

Checks for the statutory filing fee of **$ 690.00** and Assignment recordation fee of **$ 40.00** are attached. You are also directed and authorized to charge or credit any difference or overpayment to Deposit Account No. 19-4880. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. 1.16 and 1.17 and any petitions for extension of time under 37 C.F.R. 1.136 which may be required during the entire pendency of the application to Deposit Account No. 19-4880. A duplicate copy of this transmittal letter is attached.

Priority is claimed from:

Japanese Patent Application	Filing Date
P. 2000-039851	February 17, 2000

Respectfully submitted,
SUGHRUE, MION, ZINN, MACPEAK & SEAS
Attorneys for Applicant(s)

By Jean C. Edwards 41,728 for
Darryl Mexic
Registration No. 23,063

DM:maa

PROGRAMMABLE CONTROLLER

BACKGROUND OF THE INVENTION

The present invention relates to a programmable controller which performs high - speed pulse output to control a controlled apparatus for positioning control according to a user program.

Fig. 3 is a diagram showing the structure of a conventional programmable controller.

In Fig. 3, the reference numeral 1 denotes a central processing unit (which will be hereinafter referred to as a "CPU") for controlling each section of the programmable controller, and the reference numeral 2 denotes a pulse generating section for generating a pulse string in a cycle set by the CPU 1.

Figs. 4A and 4B are flowcharts showing the operation of the conventional programmable controller. Fig. 4A shows a main processing and Fig. 4B shows an interruption processing.

In the main processing shown in Fig. 4A, first of all, the CPU 1 sets an output pulse cycle of the pulse generating section 2 at Step S1 and sets a residual pulse number indicative of an output pulse number at Step S2. Then, an interrupt enable state for enabling interruption is set at Step S3 and pulse output is started at Step S4. At Step S5, pulse output for the residual pulse number is carried out. When the pulse output

is completed, an interrupt disable state is set at Step S6. Thus, the main processing is ended.

Every time one pulse is output at the Step S5, the interruption processing shown in Fig. 4B is executed. At Step S11, one is subtracted from the residual pulse number. When the residual pulse number reaches zero, a processing of stopping the pulse output is carried out at Step S13. Thus, the interruption processing is ended. If the residual pulse number is not zero at the Step S12, the interruption processing is ended and the control is returned to the main processing. By the main processing, the pulse output at the Step S5 is executed successively.

The conventional programmable controller comprises a CPU 1 for controlling each section and a pulse generating section 2 for generating a pulse string having a cycle set by the CPU 1 as shown in Fig. 3, and is controlled by control means for executing an interruption processing for each pulse output as shown in Figs. 4A and 4B. The control means sequentially subtracts one from the residual pulse number for each output pulse, and executes the processing of stopping the pulse when the residual pulse number reaches zero.

In the conventional art, the CPU 1 should execute an interruption processing for each pulse output. For example, in case where a pulse of 200 KHz is output, an interruption cycle is 5μs. Therefore, it is necessary to use a high - speed CPU

applicable to the interruption processing having a cycle of 5 μs. However, the CPU applicable to such a high - speed processing using a general one - chip microcomputer is expensive. As a result, the cost of a product is increased.

SUMMARY OF THE INVENTION

The invention has been made to solve such a problem and has an object to obtain a programmable controller which is inexpensive and can carry out high - speed pulse output.

A programmable controller according to the invention comprises a pulse generating section for outputting a pulse string having a set cycle, a pulse dividing section for dividing the pulse string output from the pulse generating section at a predetermined dividing ratio and for outputting an interruption request signal having a cycle which is n times (n is a positive integer) as great as the cycle of the pulse string, and a central processing unit for executing an interruption processing in response to the interruption request signal output from the pulse dividing section, thereby controlling the output of the pulse generating section.

Moreover, the central processing unit sets a dividing ratio to be used for division of the pulse dividing section, controls the number of pulses output from the pulse generating section and sets the dividing ratio to be equal to the number of pulses which have not been output when the number of the pulses

which have not been output is smaller than 2n.

Furthermore, the central processing unit changes the dividing ratio to be used for the division of the pulse dividing section depending on the cycle of the pulse string output from the pulse generating section.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram showing the structure of a programmable controller according to first and second embodiments of the invention;

Figs. 2A and 2B are flowcharts showing the operation of the programmable controller according to the first and second embodiments of the invention;

Fig. 3 is a diagram showing the structure of a conventional programmable controller; and

Figs. 4A and 4B are flowcharts showing the operation of the conventional programmable controller.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

(First Embodiment)

Fig. 1 is a diagram showing the structure of a programmable controller according to a first embodiment of the invention.

In Fig. 1, the reference numeral 1 denotes a CPU for controlling each section in the programmable controller, the

reference numeral 2 denotes a pulse generating section for generating a pulse string having a cycle set by the CPU 1, and the reference numeral 3 denotes a pulse dividing section for outputting, as an interruption request to the CPU 1, a signal obtained by dividing a pulse output from the pulse generating section 2 at a dividing ratio set by the CPU 1. The components 1 to 3 constitute the programmable controller. In the first embodiment, the CPU 1 controls an output pulse by control means for executing an interruption processing for each n - time pulse output.

Figs. 2A and 2B are flowcharts showing the operation of the programmable controller according to the first embodiment of the invention. Fig. 2A shows a main processing and Fig. 2B shows an interruption processing.

In the main processing shown in Fig. 2A, Steps S1 and S2 are executed in the same manner as those in Fig. 4A. Then, a pulse dividing ratio n (n is a positive integer) of the pulse dividing section 3 is set at Step S21. Subsequently, processings are executed at Steps S3 to S6 in the same manner as those in Fig. 4A.

In the interruption processing shown in Fig. 2B, n is subtracted from a residual pulse number at Step S22. Then, if the residual pulse number < 2n is satisfied at Step S23, the CPU 1 sets the pulse dividing ratio n to be equal to the residual pulse number at Step S24. Thereafter, the routine proceeds to

Step S12. If the residual pulse number < 2n is not satisfied at the Step S23, the routine proceeds to the Step S12. At the Steps S12 and S13, the same processings as those in Fig. 4B are executed.

In the first embodiment, the dividing ratio n is set to the pulse dividing section 3 by the CPU 1. Consequently, the cycle of the interruption processing is set to be n times as great as that of a pulse output from the pulse generating section 2. Therefore, the interruption processing can be executed by a CPU having a throughput of 1 / n as compared with the conventional art. For example, in case where a dividing ratio of n = 100 is set, an interruption cycle of $5\mu S \times 100 = 500\ \mu S$ is obtained for outputting a pulse of 200 KHz. Thus, it is possible to obtain an interruption cycle to which an inexpensive one - chip microcomputer is fully applicable.

When the interruption processing is executed in a cycle which is n times as great as the cycle of the output pulse, the residual pulse number in the interruption processing can be checked only for each n - pulse. Consequently, it is possible to output only a pulse having a number which is integer times as great as n. In the first embodiment, a countermeasure is taken. More specifically, when the residual pulse number is smaller than 2n, the CPU 1 causes the pulse dividing section 3 to set a dividing ratio which is equal to the residual pulse number in the interruption processing shown in the Steps S23

and S24 of Fig. 2B. Consequently, when the next interruption is carried out, the residual pulse number reaches zero and the pulse output can be stopped with an optional pulse number.

While the pulse output is carried out n times for each interruption cycle after the pulse output is started and the pulse output is carried out in a final interruption cycle fraction times which are equal to or greater than n and smaller than 2n in the first embodiment, calculation is previously executed prior to the start of the pulse output so that the pulse can be output fraction times in an initial interruption cycle and n times which are equal to or greater than two until the final interruption cycle.

(Second Embodiment)

In a second embodiment, the same structure as that illustrated in Fig. 1 is employed, and the same operation as that shown in the flowcharts of Figs. 2A and 2B is carried out.

A difference between the first and second embodiments will be described below.

In the first embodiment, the dividing ratio n has a predetermined value. If the frequency of an output pulse is increased, an interruption cycle for the CPU 1 is shortened in proportion thereto. In this case, a load on the CPU 1 is increased. Consequently, if the cycle of a pulse to be output is increased, the responsivity of processings other than the pulse output of the programmable controller is deteriorated.

In the second embodiment, a countermeasure is taken. More specifically, the dividing ratio n is varied corresponding to the cycle of an output pulse. Consequently, even if the cycle of the output pulse is varied, a constant interruption cycle for the CPU 1 is maintained.

In the second embodiment, the constant interruption cycle for the CPU 1 is maintained irrespective of a change in an output frequency. Therefore, even if the output pulse cycle is increased, the responsitivity of the processings other than the pulse output is not deteriorated.

Since the invention has the above-mentioned structure, the following effects can be obtained.

The programmable controller according to the invention comprises a pulse generating section for outputting a pulse string having a set cycle, a pulse dividing section for dividing the pulse string output from the pulse generating section at a predetermined dividing ratio and for outputting an interruption request signal having a cycle which is n times (n is a positive integer) as great as the cycle of the pulse string, and a central processing unit for executing an interruption processing in response to the interruption request signal output from the pulse dividing section, thereby controlling the output of the pulse generating section. Consequently, the cycle of the interruption processing can be increased, and the central processing unit having a low throughput is applicable

to the interruption processing.

Moreover, the central processing unit sets a dividing ratio to be used for division of the pulse dividing section, controls the number of pulses output from the pulse generating section and sets the dividing ratio to be equal to the number of pulses which have not been output when the number of the pulses which have not been output is smaller than 2n. Therefore, a pulse which has not been output can be output in the final interruption processing.

Furthermore, the central processing unit changes the dividing ratio to be used for the division of the pulse dividing section depending on the cycle of the pulse string output from the pulse generating section. Consequently, an interruption processing having a cycle suitable for the central processing unit can be executed irrespective of the cycle of a pulse to be output.

WHAT IS CLAIMED IS:

1. A programmable controller for controlling a controlled apparatus by pulse output, comprising:

a pulse generating section for outputting a pulse string having a set cycle,

a pulse dividing section for dividing the pulse string output from said pulse generating section at a predetermined dividing ratio and for outputting an interruption request signal having a cycle which is n times (n is a positive integer) as great as the cycle of the pulse string, and

a central processing unit for executing an interruption processing in response to the interruption request signal output from said pulse dividing section so as to control the output of said pulse generating section.

2. The programmable controller according to claim 1, wherein said central processing unit sets a dividing ratio to be used for division of the pulse dividing section, controls the number of pulses output from said pulse generating section, and sets the dividing ratio to be equal to the number of pulses which have not been output when the number of the pulses which are output is smaller than 2n.

3. The programmable controller according to claim 1, wherein said central processing unit changes the dividing ratio to be used for the division of said pulse dividing section depending on the cycle of the pulse string output from said pulse generating section.

ABSTRACT OF THE DISCLOSURE

An output cycle of a pulse string generated from a pulse generating section (2) is divided by a pulse dividing section (3) and a signal having a cycle which is plural times as great as the cycle of an output pulse is output from the pulse dividing section (3). This signal is input as an interruption request signal to a CPU (1). Consequently, the CPU (1) can execute an interruption processing in a cycle which is plural times as great as the cycle of the output pulse. By the interruption processing, the number of pulses to be output is controlled.

FIG. 1

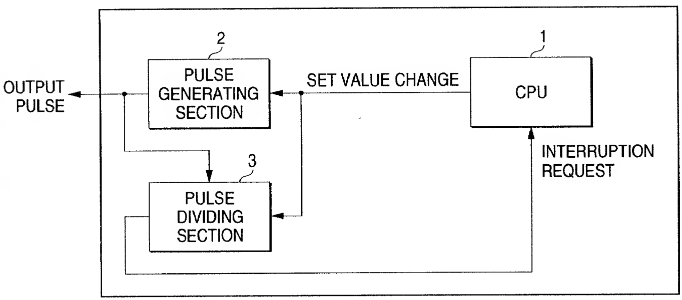

2
PULSE GENERATING SECTION
1
CPU
SET VALUE CHANGE
OUTPUT PULSE
3
PULSE DIVIDING SECTION
INTERRUPTION REQUEST

FIG. 2A

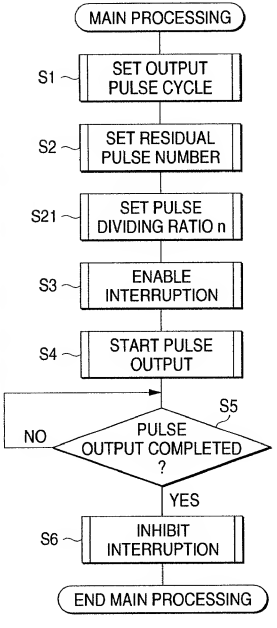


FIG. 2B

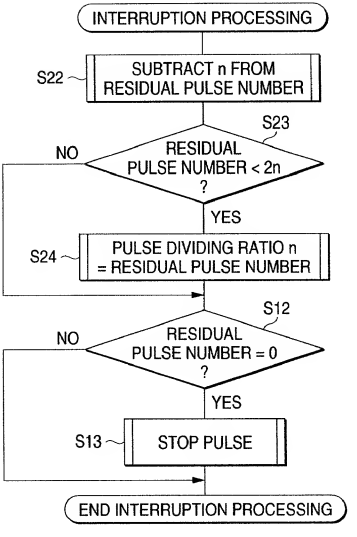


FIG. 3

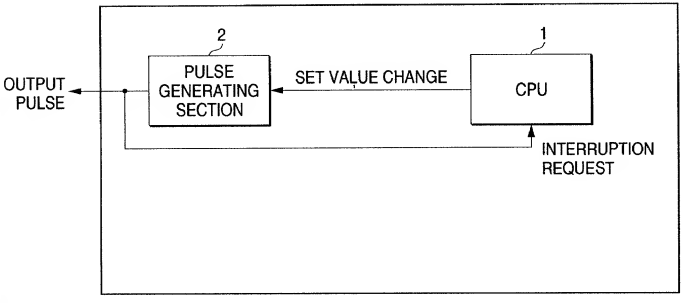

2
1
OUTPUT PULSE
PULSE GENERATING SECTION
SET VALUE CHANGE
CPU
INTERRUPTION REQUEST

FIG. 4A

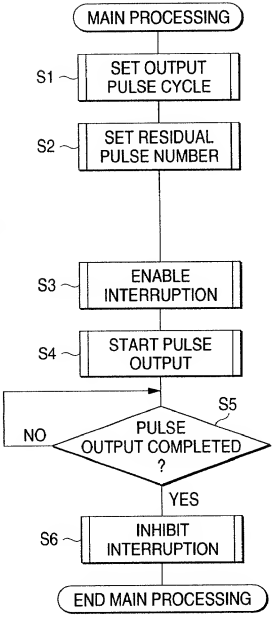
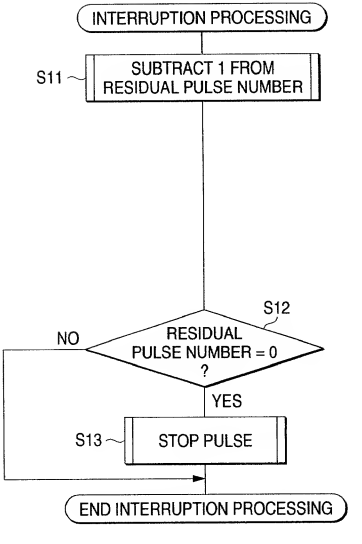

MAIN PROCESSING
S1
SET OUTPUT PULSE CYCLE
S2
SET RESIDUAL PULSE NUMBER
S3
ENABLE INTERRUPTION
S4
START PULSE OUTPUT
S5
NO
PULSE OUTPUT COMPLETED ?
YES
S6
INHIBIT INTERRUPTION
END MAIN PROCESSING

FIG. 4B


INTERRUPTION PROCESSING
S11
SUBTRACT 1 FROM RESIDUAL PULSE NUMBER
S12
NO
RESIDUAL PULSE NUMBER = 0 ?
YES
S13
STOP PULSE
END INTERRUPTION PROCESSING

Declaration and Power of Attorney for Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name,

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

[redacted]

PROGRAMMABLE CONTROLLER

上記発明の明細書（下記の欄でX印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

～ ___月___日に提出され、米国出願番号または特許協定条約

国際出願番号を _____ とし、

（該当する場合） _____ に訂正されました。

~ was filed on _____
as United States Application Number or
PCT International Application Number

_____ and was amended on

_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration

（日本語宣言書）

私は、米国法典第35編第119条(a)-(d)項又は第365条(b)項に基き下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約第365条(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Applications 外国での先行出願			Priority Not Claimed 優先権主張なし
P. 2000-039851	Japan	17/February/2000	☐
(Number) （番号）	(Country) （国名）	(Day/Month/Year Filed) （出願年月日）	
			☐
(Number) （番号）	(Country) （国名）	(Day/Month/Year Filed) （出願年月日）	
			☐
(Number) （番号）	(Country) （国名）	(Day/Month/Year Filed) （出願年月日）	

私は、第35編米国法典119条(e)項に基づいて下記の米国特許出願規定に記載された権利をここに主張致します。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) （出願番号）	(Filing Date) （出願日）	(Application No.) （出願番号）	(Filing Date) （出願日）

私は、下記の米国法典第35編第120条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約第365条(c)に基づく権利をここに主張します。又、本出願の各請求範囲の内容が米国法典第35編第112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内又は特許協力条約国際出願提出日までの期間中に入手された、連邦規則法典第37編第1条第56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit of Title 35, United States Code Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose any material information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況：特許許可済、係属中、放棄済）
(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況：特許許可済、係属中、放棄済）

私は、私自身の知識に基づいて本宣言中で私が行う表明が真実であり、かつ私の入手した情報と私の信ずるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行えば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

（日本語宣言書）

委任状：私は、下記の発明者として、本出願に関する一切の手続きを米国特許商標局に対して遂行する弁理士又は代理人として、下記のものを指名致します。（弁護士、又は代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

John H. Mion, Reg. No. 18,879; Thomas J. Macpeak, Reg. No. 19,292; Robert J. Seas, Jr., Reg. No. 21,092; Darryl Mexic, Reg. No. 23,063; Robert V. Sloan, Reg. No. 22,775; Peter D. Olexy, Reg. No. 24,513; J. Frank Osha, Reg. No. 24,625; Waddell A. Biggart, Reg. No. 24,861; Louis Gubinsky, Reg. No. 24,835; Neil B. Siegel, Reg. No. 25,200; David J. Cushing, Reg. No. 28,703; John R. Inge, Reg. No. 26,916; Joseph J. Ruch, Jr., Reg. No. 26,577; Sheldon I. Landsman, Reg. No. 25,430; Richard C. Turner, Reg. No. 29,710; Howard L. Bernstein, Reg. No. 25,665; Alan J. Kasper, Reg. No. 25,426; Kenneth J. Burchfiel, Reg. No. 31,333; Gordon Kit, Reg. No. 30,764; Susan J. Mack, Reg. No. 30,951; Frank L. Bernstein, Reg. No. 31,484; Mark Boland, Reg. No. 32,197; William H. Mandir, Reg. No. 32,156; Scott M. Daniels, Reg. No. 32,562; Brian W. Hannon, Reg. No. 32,778; Abraham J. Rosner, Reg. No. 33,276; Bruce E. Kramer, Reg. No. 33,725; Paul F. Neils, Reg. No. 33,102 and Brett S. Sylvester, Reg. No. 32,765

書類送付先：

Send Correspondence to:

SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC
2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037-3213

直通電話連絡先：（名称及び電話番号）

Direct Telephone Calls to: ***(name and telephone number)***

(202)293-7060

唯一又は第一発明者名	Full name of sole or first inventor **Shinsuke YOKOKAWA**
発明者の署名　日付	Inventor's signature　Date Shinsuke Yokokawa **July 18,2000**
住所	Residence **Tokyo, Japan**
国籍	Citizenship **Japan**
郵便の宛先	Post office address **c/o Mitsubishi Denki Kabushiki**
	Kaisha, 2-3, Marunouchi 2-chome, Chiyoda-ku, TOKYO 100-8310 JAPAN
第二共同発明者名（該当する場合）	Full name of second joint inventor, if any
第二発明者の署名　日付	Second inventor's signature　Date
住所	Residence
国籍	Citizenship
郵便の宛先	Post office address

（第三以降の共同発明者についても同様に記載し、署名をすること。）

(Supply similar information and signature for third and subsequent joint inventors.)